EE480 Assignment 1: 8-bit Signed Saturation Adder

Implementor's Notes

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ABSTRACT

This project was a simple combinatorial design problem to ensure that students were somewhat comfortable with basic use of Verilog, including the concept of writing an exhaustive testbench.

1. GENERAL APPROACH

This assignment required construction of a synthesizable 8-bit signed saturation adder. It was hinted that this could be constructed using a conventional (modular) adder followed by a check for the inputs having the same sign while the output had a different sign. When that check is true, I realized that the ordinary add sign being 1 meant the saturated value should be 127, and if it is 0, the saturation result should be -128.

I built my saturation adder using three modules, `satadd8` (as required by the assignment), `add8`, and `fa`. The modular adder (`add8`) is a simple ripple-carry implementation built using full adders (`fa`).

Rather than clutter the `testbench` routine with the computation of the correct (oracle) result, I wrote a separate module for that, called `refsatadd8` – which uses the same algorithm as the sample code in the assignment.

2. ISSUES

It was a little confusing how each variable should be declared and when it should be updated.... The `#1` in `testbench` is a hack to ensure that each pair of inputs is processed in sequence with nothing missed. There are various other ways to do this, but I didn't want to implement a clock for testing what is inherently a combinatorial circuit.

Everything was tested and apparently worked correctly the first time it made it through the WWW-form compiler and simulator. However, to confirm that the error detection code in `testbench` worked, I deliberately introduced an error (an incorrect carry of `cout[2]` into `fa4`) and observed the output stating 52,744 correct and 12,792 failed. The assignment did not make clear what format the faulty outputs should be listed in, so I just composed a format where each line starts with `Wrong:`.

ACM ISBN N.A..
DOI: N.A.